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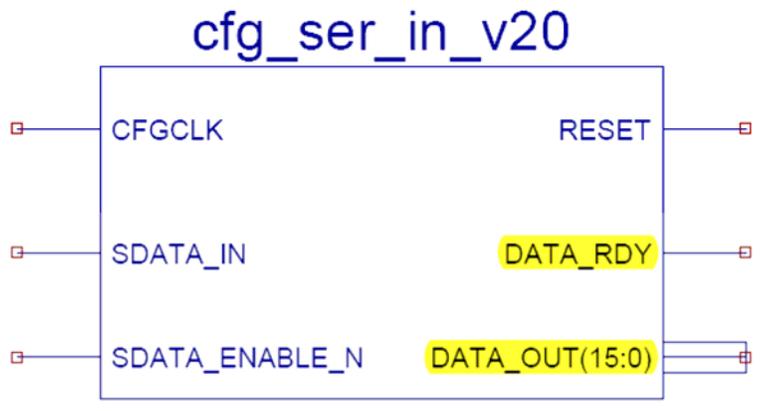
-- DESCRIPTION:

-- This module receives the ADC serial data coming from the CFG CPLD and
-- converts it into parallel data for to store it in the tel_data_mem
-- module.

-- Incoming data (SDATA_IN) is clocked in during SDATA_ENABLE high.
-- After 12 bits are received (the length of the data stream), the data
-- is available at DATA_OUT, and DATA_RDY is set.
--

-- IMPLEMENTATION NOTES:

-- Serial data should be clocked in with the falling edge of SDATA_CLK



```
CFGCLK      : in std_logic;
RESET       : in std_logic;
SDATA_IN    : in std_logic;
SDATA_ENABLE_N : in std_logic;
DATA_OUT    : out std_logic_vector(15 downto 0);
DATA_RDY    : out std_logic
```

```
type statetype is (idle, rx_data);
signal state : statetype;
signal par_reg : std_logic_vector(15 downto 0);
```

```
DATA_OUT <= par_reg;
```

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process(CFGCLK, RESET)

